**Differentiate between PLA and PAL. Explain 4-bit magnitude comparator.**

**Solution:**

The **Difference between PAL and PLA** mainly includes **PAL and PLA full form**, construction, availability, flexibility, cost, number of functions, and speed which are discussed below.

| Programmable Array Logic (PAL) | Programmable Logic Array (PLA) |
|---|---|
| The full form of PAL is programmable array logic | The full form of the PLA is a programmable logic array |
| The construction of PAL can be done using the programmable collection of AND & OR gates | The construction of PLA can be done using the programmable collection of AND & fixed collection of OR gates. |
| The availability of PAL is less prolific. | The availability of PLA is more prolofic and readily available. |
| The flexibility of PAL programming is more | The flexibility of PLA programming is less |
| The cost of a PAL is expensive | The cost of PLA is middle range |
| The number of functions implemented in PAL is large | The number of functions implemented in PLA is limited |
| The speed of PAL is slow | The speed of PLA is high |

A comparator used to compare two binary numbers each of four bits is called a 4-bit magnitude comparator. It consists of eight inputs each for two four bit numbers and three outputs to generate **less than, equal to and greater than** between two binary numbers.

In a 4-bit comparator the condition of A>B can be possible in the following four cases:

1. If A3 = 1 and B3 = 0
2. If A3 = B3 and A2 = 1 and B2 = 0
3. If A3 = B3, A2 = B2 and A1 = 1 and B1 = 0
4. If A3 = B3, A2 = B2, A1 = B1 and A0 = 1 and B0 = 0

Similarly the condition for A<B can be possible in the following four cases:

1. If A3 = 0 and B3 = 1
2. If A3 = B3 and A2 = 0 and B2 = 1
3. If A3 = B3, A2 = B2 and A1 = 0 and B1 = 1
4. If A3 = B3, A2 = B2, A1 = B1 and A0 = 0 and B0 = 1

The condition of A=B is possible only when all the individual bits of one number exactly coincide with corresponding bits of another number.

$$\therefore (A = B) = x_3 x_2 x_1 x_0$$
$$\therefore (A > B) = A_3 \overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$$
$$\therefore (A < B) = \overline{A_3} B_3 + x_3 \overline{A_2} B_2 + x_3 x_2 \overline{A_1} B_1 + x_3 x_2 x_1 \overline{A_0} B_0$$

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below:

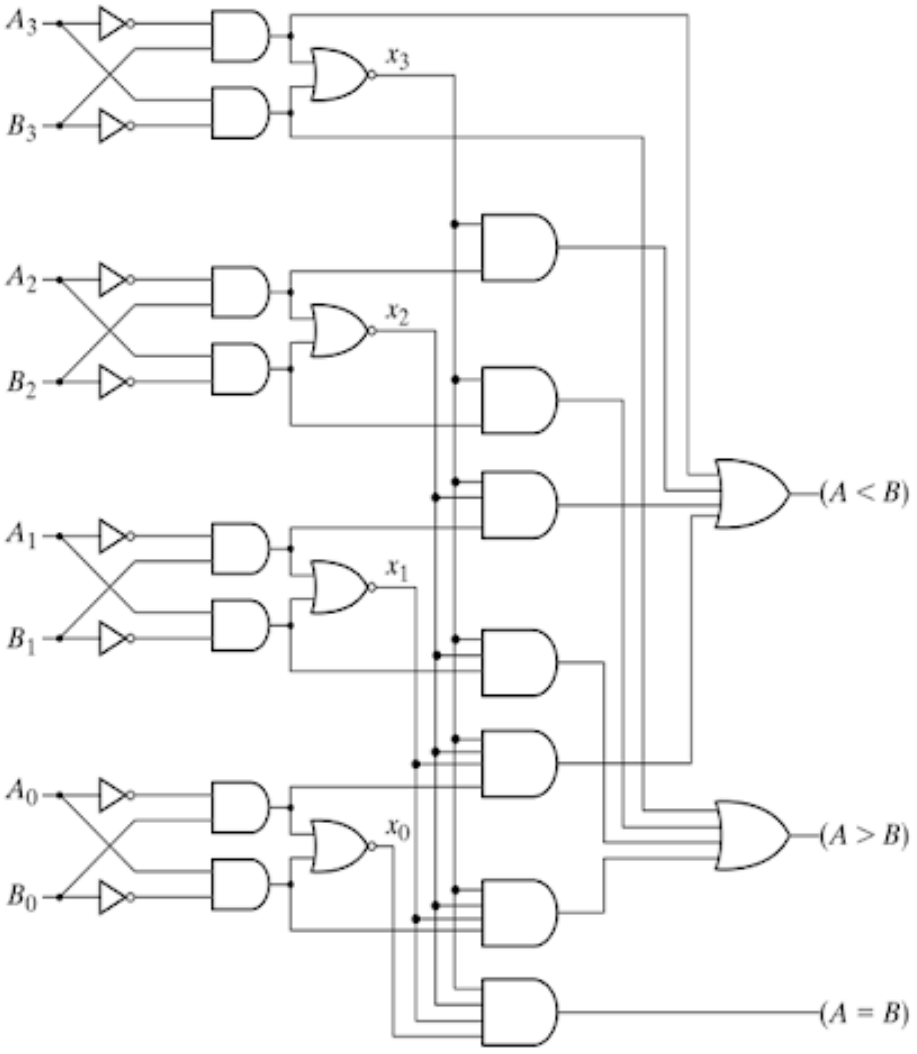


Fig. 4-17 4-Bit Magnitude Comparator